Battlezone Signature Analysis Guide ** beta 2 12-12-2015**

Thanks to Peter Fyfe for producing the original documents for Asteroids and Asteroids Deluxe upon which this guide is based. His setup info is included here for reference.

Introduction

This guide is intended as an aid to troubleshooting the ~~Asteroids~~ (ED: Battlezone) video game PCB. The Signature Analyzer used to produce this guide was an HP5004a. If it is found that the signatures hold up for other makes/models of Signature Analyzers then please let me know and I can add some kind of compatibility list to the document.

To get the most out of the guide you'll need:

Signature Analyzer (HP5004a)
Schematics for ~~Asteroids~~ (ED: Battlezone)
6502 NOP card (See the separate document 6502NOP for instructions on how to build your own NOP card)
IC Clips
Some jumper wires (3 or 4 should be sufficient)

The scope of the guide is limited in that it will not enable you to fault find the entire PCB. It should, however, be good for the following sections of the PCB:

Address Bus Buffers, Address Decoding Circuitry, Clock Circuit, Program ROMs and Data Buffer, Vector Generator Address Selector, Vector Generator RAM Select, Vector Generator ROMs and the Vector Generator Data Buffer.

The Clock Circuit test is very limited. The reason being is that I much prefer to check the clock chain with a scope. If you want to figure out the signatures for the Clock Circuit then pass on the information and I'll include it in the document. If you want a detailed description of these sections (and more) please refer to the ~~Asteroids~~ (ED: Battlezone) schematic / drawing package.

Using The Guide

For those of you who have used Atari Signature Analysis guides before then this should look familiar and there's probably no need to read through this section. For the rest of you, here's a quick run down. Every section should start with the settings for the Analyzer, something like this

setup 1

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N3-25	(CPU)
Stop	-ve	L/M/N3-25	
Clock	-ve	L/M/N3-39	φ2

The probe column refers to either the Start, Stop or Clock probes from the Signature Analyzer. The trigger column sets up the Start/Stop/Clock buttons on the front of the Analyzer. I have used –ve to indicate the negative going edge of the pulse (or the falling edge). I have used +ve to indicate the positive going edge of the pulse (or the rising edge). The IC Pin column refers to the point where the appropriate probe should be attached. The Test point column refers to an equivalent Test Point on the boards where the probe may be attached.

For example, in the example above the Start probe should be connected to pin 25 of IC L/M/N3. The Start button on the front of the Analyzer should be in the fully out position to indicate a positive going edge. Similarly, the Stop probe should be connected to the same IC/Pin as the Start probe but the Stop button on the Analyzer should be pressed in to indicate a negative going edge.

The section immediately following the set up procedure contains the signatures for that part of the test. The same structure for the Set Up was employed as explained below.

signatures 1

Probe	Signal name	Signature
K3-20	+5v	0003
K3-7	AB0	UUUU
K3-3	AB1	FFFF

Here, with the Analyzer probe on pin 20 of IC C1 you should get a reading of 0003. On pin 9 of IC C1 you should get a reading of UUUU. And so on.
A signature denoted by an (*) indicates that signature may be unstable. Try taking the signature with a 1Kohm resistor connected between the probe tip and +5V.

Down To Business
One of the things I like about this testing method is that you don't need to have the PCB in the cabinet. If you prefer to work in the back of the cabinet then that's fine. If you have a bench/test area with a +5V PSU (as I'm sure most of you have), then you can sit comfortably

at the bench. Simply connect Ground (pins 1 and 22 on the edge connector) and +5V (pins 2 and 21 on the edge connector) to the PCB, remove the game MPU and replace it with your NOP card and you're ready to start.
Just set up the Analyzer as indicated and start probing for those signatures. Always remember to have the Watchdog disabled as this will lead to permanently unstable signatures.

What To Do When You Find An Incorrect Signature
If you find a signature that doesn't match the guide, check your set up first. If your set up is OK then you'll need to trace the fault. Rather than having a long winded ramble from me it would be better to look at the following link on Al Kossow's page. If you haven't already had a look at his site then I'd definitely recommend having a look as it's a bit of a gold mine.
http://www.spies.com/arcade/TE/SigAnalNotes.pdf
After you've had a look through the document then you should know enough to start tracing the fault. It should also give you a bit more information on Signature Analysis in general.

Some Common Faults
The two most common faults I've come across are bad sockets and shorted traces. During the Signature Analysis the bad socket problem is highlighted by the fact that the signatures are unstable. You may get some stable and some not. When you get unstable signatures whilst doing the ROM tests it does not necessarily indicate a bad ROM. Reseating the ROM or replacing the socket is usually a good place to start. The problem of shorted traces is usually down to something being dragged across the board. Sometimes they can be quite hard to see but Signature Analysis shows it up quite good.

Disclaimer
If you toast yourself, your house, your dog, your family or more importantly your video game, then it's not my fault. You use the information contained in this guide at your own risk. Good luck.

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*** Tie the Watchdog Disable test point to ground for all tests. ***

1. Address Lines

Address Buffer Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N3-25	(CPU)
Stop	-ve	L/M/N3-25	
Clock	-ve	L/M/N3-39	φ2

signatures

Probe	Signal name	Signature
K3-20	+5v	0003
K3-18	AB0	UUUU
K3-3	AB1	FFFF
K3-16	AB2	8484
K3-5	AB3	P763
K3-14	AB4	1U5P
K3-7	AB5	0356
K3-12	AB6	U759
K3-9	AB7	6F9A
N2-18	AB8	7791
N2-16	AB9	6321
N2-14	AB10	37C5
N2-12	AB11	6U28
N2-9	AB12	4FCA
L/M/N3-23	A13	4868
L/M/N3-24	A14	9UP1
L/M/N3-25	A15	0001

2. Address Decoding

Address Decoder Test

setup 1

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N-3	
Stop	-ve	L/M/N3-25	
Clock	-ve	L/M/N3-39	φ2

signatures 1

Probe	Signal name	Signature
K5-4	SINP	H889
K5-5	OPT0	A0U3
K5-6	OPT1	U389
M2-4		P508
M2-5	VMEM	7APA
M2-6	PMEML	AH63
M2-7	PMEMH	3282
M2-9	ROM5	86C1
M2-10	ROM4	A04H
M2-11	ROM3	UH4P
M2-12	ROM2	P933
L2-8	ROM1	8756
L2-6	ROM0	2A36
C4-5		9A53
C4-7	I/O	0H06
J5-3		9A53

setup 2

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N-3	
Stop	-ve	L/M/N3-25	
Clock	-ve	N4-3	6MHz

** tie R/W test point to ground **

signatures 2

Probe	Signal name	Signature
C4-16	+5v	00UP
C4-4	RAM	9CC8
C4-6		49UH
C4-7	I/O	4F9F
J5-11		6CUP
K5-9	DMACNT	U51U
K5-10	WDCLR	20H3
K5-11	DMAGO	FUC0

** remove R/W ground jumper **

3. Watchdog Circuit

Watchdog Circuit Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N3-25	(CPU)
Stop	-ve	L/M/N3-25	
Clock	-ve	L/M/N3-39	φ2

** tie K5-6 to ground **

signatures

Probe	Signal name	Signature
J4-14	+5v	0003
J4-1		0003
H4-6		0003
H4-8		0000

** remove K5-6 ground jumper **

4. Clock Circuit

Clock Circuit Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	L/M/N3-25	(CPU)
Stop	-ve	L/M/N3-25	
Clock	-ve	L/M/N3-39	φ2

** tie K5-6 to ground **

signatures

Probe	Signal name	Signature
N5-6		763H
N5-8	3MHz	8A4U
N5-10	12MHz	9720

5. ROM and Data Lines

ROM0 Test (E1)

setup E1

Probe	Trigger	IC Pin	Test point
Start	-ve	L2-6	
Stop	+ve	L2-6	
Clock	-ve	L/M/N3-39	φ2

signatures E1

Probe	Signal name	Signature
E1-24	+5V	826P
E1-9	DB0	9A15 or 363C
E1-10	DB1	8P38 or 25HC
E1-11	DB2	1U20 or 8A53
E1-13	DB3	A782 or 58H9
E1-14	DB4	38AP or 32C3
E1-15	DB5	3F18 or 8285
E1-16	DB6	16A4 or 8848
E1-17	DB7	H7AA or A69A

ROM1 Test (F/H1)

setup F/H1

Probe	Trigger	IC Pin	Test point
Start	-ve	L2-8	
Stop	+ve	L2-8	
Clock	-ve	L/M/N3-39	φ2

signatures F/H1

Probe	Signal name	Signature
F/H1-24	+5V	826P
F/H1-9	DB0	P424
F/H1-10	DB1	787P
F/H1-11	DB2	66H1
F/H1-13	DB3	2PP5
F/H1-14	DB4	UP54
F/H1-15	DB5	A776
F/H1-16	DB6	1FU9
F/H1-17	DB7	F06P

ROM2 Test (J1)

setup J1

Probe	Trigger	IC Pin	Test point
Start	-ve	M2-12	
Stop	+ve	M2-12	
Clock	-ve	L/M/N3-39	φ2

signatures J1

Probe	Signal name	Signature
J1-24	+5V	826P
J1-9	DB0	0CC5
J1-10	DB1	UA92
J1-11	DB2	366F
J1-13	DB3	C07U
J1-14	DB4	P29A
J1-15	DB5	52A8
J1-16	DB6	6267
J1-17	DB7	F6AA

ROM3 Test (K1)

setup K1

Probe	Trigger	IC Pin	Test point
Start	-ve	M2-11	
Stop	+ve	M2-11	
Clock	-ve	L/M/N3-39	φ2

signatures K1

Probe	Signal name	Signature
K1-24	+5V	826P
K1-9	DB0	C295
K1-10	DB1	7H94
K1-11	DB2	836U
K1-13	DB3	6AH4
K1-14	DB4	0656
K1-15	DB5	CUAC
K1-16	DB6	F1A8
K1-17	DB7	UUAF

ROM4 Test (L/M1)

setup L/M1

Probe	Trigger	IC Pin	Test point
Start	-ve	M2-10	
Stop	+ve	M2-10	
Clock	-ve	L/M/N3-39	φ2

signatures L/M1

Probe	Signal name	Signature
L/M1-24	+5V	826P
L/M1-9	DB0	8UP2
L/M1-10	DB1	940C
L/M1-11	DB2	0884
L/M1-13	DB3	2900
L/M1-14	DB4	C1FA
L/M1-15	DB5	923H
L/M1-16	DB6	112U
L/M1-17	DB7	H08P

ROM5 Test (N1)

setup N1

Probe	Trigger	IC Pin	Test point
Start	-ve	M2-9	
Stop	+ve	M2-9	
Clock	-ve	L/M/N3-39	φ2

signatures N1

Probe	Signal name	Signature
N1-24	+5V	826P
N1-9	DB0	8549
N1-10	DB1	UPH7
N1-11	DB2	2260
N1-13	DB3	8F75
N1-14	DB4	3ACA
N1-15	DB5	3P22
N1-16	DB6	PAPA
N1-17	DB7	C001

6. Data Buffer

Data Buffer Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	M2-12	
Stop	+ve	M2-12	
Clock	-ve	L/M/N3-39	φ2

signatures

Probe	Signal name	Signature
P2-20	+5V	826P
P2-18	D0	P29A
P2-17	D1	C07U
P2-16	D2	52A8
P2-15	D3	6267
P2-14	D4	F6AA
P2-13	D5	366F
P2-12	D6	UA92
P2-11	D7	0CC5

7. Vector Generator Address Selector

Vector Generator Address Selector Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	L/MN3-25	
Stop	-ve	L/MN3-25	
Clock	-ve	L/M/N3-39	φ2

** tie D4-1 to ground **

signatures

Probe	Signal name	Signature
C4-16	+5V	0003
C4-9	VROM3	89CC
C4-10	VROM2	F501
C4-11	VROM1	P693
H4-9	AM0	8484
H4-7	AM1	UUUU
H4-4	AM2	FFFF

H4-12	AM3	P763
F4-12	AM4	6F9A
F4-4	AM5	0356
F4-7	AM6	1U5P
F4-9	AM7	U759
E4-9	AM8	7791
E4-12	AM9	6321
E4-4	AM10	37C5
D4-4	AM11	6U28
D4-12	AM12	4FCA

8. Vector Generator RAM

Vector Generator RAM Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	L/MN3-25	
Stop	-ve	L/MN3-25	
Clock	-ve	L/M/N3-39	φ2

** tie D4-1 to ground **

signatures

Probe	Signal name	Signature
B4-16	+5V	0003
B4-1	VRAM0	32U8
B4-2	VRAM1	98H1
B4-3	VRAM2	59C9
B4-4	VRAM3	CU29

8. Vector Generator ROM

VROM2 Test (B/C3)

setup B/C3

Probe	Trigger	IC Pin	Test point
Start	-ve	C4-10	VROM2
Stop	+ve	C4-10	VROM2
Clock	-ve	L/M/N3-39	φ2

** tie D4-1 to ground **

signatures B/C3

Probe	Signal name	Signature
B/C3-24	+5V	826P
B/C3-9	DVG0	H90F
B/C3-10	DVG1	CCHU
B/C3-11	DVG2	HP85
B/C3-13	DVG3	P931
B/C3-14	DVG4	588C
B/C3-15	DVG5	1560
B/C3-16	DVG6	8C2P
B/C3-17	DVG7	5114

VROM3 Test (A3)

setup A3

Probe	Trigger	IC Pin	Test point
Start	-ve	C4-9	VROM3
Stop	+ve	C4-9	VROM3
Clock	-ve	L/M/N3-39	φ2

** tie D4-1 to ground **

signatures A3

Probe	Signal name	Signature
A3-24	+5V	826P
A3-9	DVG0	F2HA
A3-10	DVG1	A427
A3-11	DVG2	UH32
A3-13	DVG3	CUA2
A3-14	DVG4	H151
A3-15	DVG5	7UF4
A3-16	DVG6	U55H
A3-17	DVG7	1A43

8. Vector Generator Data Buffer

Vector Generator Data Buffer Test

setup

Probe	Trigger	IC Pin	Test point
Start	-ve	C4-10	VROM3
Stop	+ve	C4-10	VROM3

Clock	-ve	L/M/N3-39	φ2

** tie D4-1 to ground **

signatures

Probe	Signal name	Signature
F2-20	+5V	826P
F2-18	DVG0	F2HA
F2-17	DVG1	A427
F2-16	DVG2	UH32
F2-15	DVG3	CUA2
F2-14	DVG4	H151
F2-13	DVG5	7UF4
F2-12	DVG6	U55H
F2-11	DVG7	1A43